

Drill Table: Top Layer to Bottom Layer

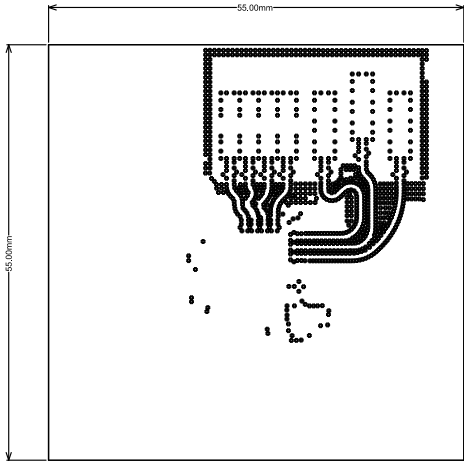
Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length	Drill Layer Pair
⊕	981	5.90mil (0.150mm)	PTH	Round	-	-	Top Layer - L2
	981 Total						

FOR PTH +/- 3MIL  
FOR NPTH +/- 2MIL  
FOR 7.874MIL DRILL +0/-7.874MIL  
FOR 10MIL DRILL +0/-10MIL  
FOR 12.2MIL DRILL +0/-12.2MIL

Drill Table: Layer 1 To Layer 2

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length	Drill Layer Pair
⊕	981	5.90mil (0.150mm)	PTH	Round	-	-	Top Layer - L2
	981 Total						

FOR 5.9MIL DRILL +0/-5.9MIL



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC073	REV: B	SUN REV: Not In VersionControl
LAYER NAME = Drill Drawing	TID #: N/A		
PLOT NAME = Fabrication Drawing-1	GENERATED : 11/28/2018 8:09:20 PM	TEXAS INSTRUMENTS	

### Drill Table: Top Layer to Bottom Layer

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length	Drill Layer Pair
✖	9	7.87mil (0.200mm)	PTH	Round	-	-	Top Layer - Bottom Layer
✱	89	10.00mil (0.254mm)	PTH	Round	-	-	Top Layer - Bottom Layer
▼	335	12.20mil (0.310mm)	PTH	Round	-	-	Top Layer - Bottom Layer
◇	4	40.16mil (1.020mm)	NPTH	Round	-	-	Top Layer - Bottom Layer
●	1	80.00mil (2.032mm)	PTH	Round	-	-	Top Layer - Bottom Layer
■	8	118.11mil (3.000mm)	PTH	Round	-	-	Top Layer - Bottom Layer
	446 Total						

FOR PTH +/- 3MIL  
FOR NPTH +/- 2MIL  
FOR 7.874MIL DRILL +0/-7.874MIL  
FOR 10MIL DRILL +0/-10MIL  
FOR 12.2MIL DRILL +0/-12.2MIL

### Drill Table: Layer 1 To Layer 2

FOR 5.9MIL DRILL +0/-5.9MIL

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.80mil	1	
3	Top Layer	Copper	1.60mil		
4	Dielectric 1	RO4835 LOPRO	4.00mil	3.66	
5	L2	Copper	1.40mil		
6	Dielectric 2	1080 (66)X2 370HR	5.67mil	3.9	
7	L3	Copper	1.20mil		
8	Dielectric 3	4-7628 370HR	28.00mil	4.36	
9	L4	Copper	1.20mil		
10	Dielectric 4	1080 (66)X2 370HR	5.90mil	3.9	
11	L5	Copper	1.20mil		
12	Dielectric 5	1-2166 370HR	4.00mil	4.26	
13	Bottom Layer	Copper	1.60mil		
14	Bottom Solder	Solder Resist	0.80mil	1	
15	Bottom Overlay				

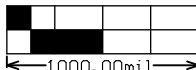
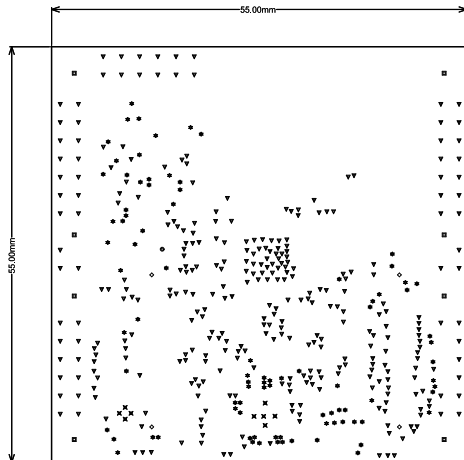
## IMPEDANCE TABLE

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP	7.795 MILS	8 MILS	50 OHM	LAYER-2 (GND LAYER)

LAYER	TRACE WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE LAYER
TOP AND BOTTOM	5.2 MILS	5 MILS	100 OHM	LAYER-2 AND LAYER-5

NOTES:

1. THIS IS AN IMPEDANCE CONTROL BOARD
2. VIA'S ON PAD AND BGA PACKAGE AREA SHOULD BE FILLED WITH CONDUCTIVE MATERIAL AND SURFACE SHOULD BE FLAT  
BGA AREA VIAS SHOULD BE CAPPED WITH COPPER PLATING TO ENSURE FLAT SURFACE  
FLATNESS TOLERANCE FOR VIA ON PADS: +0.000 /- 0.001 INCHES ON BOTH SIDES.  
OTHER THAN BGA AND VIA'S ON THE PAD VIA FILLING REQUIREMENT CAN BE EXEMPTED
3. SOLDER MASK OPENING IS KEPT SAME SIZE AS PAD (1:1)  
THE MANUFACTURER IS REQUESTED TO RESIZE IT AS PER THEIR SOLDERMASK TOLERANCE EXCEPT NPTH DRILL AND FIDUCIALS.
4. VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
5. MANUFACTURER'S IDENTIFICATION,DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
6. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL
7. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-2 MIL
8. REFER IMPEDANCE TABLE FOR IMPEDANCE CONTROL TRACES ON LAYER 1 AND LAYER 6.
9. FOR ACCURACY OF THE ANTENNA DIMENSION, NEED TO BE MEASURE THE ANTENNA DIMENSIONS ON ONE BOARD AS PER ANTENNA DOCUMENT( Visio-IWR\_60GHz4).
10. INTENTIONAL ONE NET ANTENNA VIA IS PRESENT IN DESIGN



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC073	REV: B	SVN REV: Not In VersionControl
LAYER NAME = 0205-Substrates	TID #: N/A		
PLOT NAME = Fabrication Drawing-2	GENERATED : 11/28/2018 8:09:26 PM		TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

DESIGN INFORMATION

MIN. TRACK WIDTH: 4 MIL  
MIN. CLEARANCE: 4 MIL  
MIN. VIA PAD SIZE: 13.22 MIL

MINIMUM ANNULAR RING 0.099mm (3.9MIL) EXTERNAL  
PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL; HOLES +/- 3 MIL  
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: ☐ FR-408 ☐ FR-4 High Tg ☒ OTHER \_\_\_\_\_

THICKNESS: ☐ 62 MIL (1.6mm) +/-10% ☒ OTHER 57.37 MIL +/-10%

TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/- \_\_\_\_\_

BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2  
☐ OTHER +/- \_\_\_\_\_

DRILLING:  
REFERENCE: ☒ AS SHOWN ☒ NC\_DRILL FILES  
PTH COPPER THICKNESS: ☒ 20-30  $\mu$ m ☐ OTHER

BOARD FINISH:  
SILKSCREEN: ☒ TOP ☒ BOTTOM  
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER \_\_\_\_\_  
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED  
☐ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☐ IMMERSION GOLD (ENIG) ☐ ENEPIG  
☒ IMM. TIN/SILVER OR EQUIV ☐ OTHER \_\_\_\_\_

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE  
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs  
TO MEET OR EXCEED THE REQUIREMENTS OF:  
☒ ANSI PC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3  
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:  
MICROSECTION: ☐ YES

BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER

☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE

☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE

☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE

☐ LAYER 1 & 6 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE

☐ TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE



PROJECT TITLE: IWR6843ISK<Industrial Starter Kit>
DESIGNED FOR: Public Release
FILE NAME: PROC073B_PCB.PcbDoc

ENGINEER: Chethan Kumar Y.B	LAYOUT BY: Tessolve
SCALE: 1.00	ALTUM DESIGNER VERSION: 17.1.9.592